SCHEME – E

Sample Question Paper

Course Name : Electronics Engineering Groups

Course Code : EJ/EN/EX/IS/MU/IE/IC/DE/EV/ED/EI

Semester : Third

12069

Subject Title : Principles of Digital Techniques

Marks : 100 **Time: 3 Hours**

Instructions: 1] All questions are compulsory.
2] Figures to the right indicates full marks.
3] Use of non-programmable calculator is permissible.

Q.1 Attempt any TEN of the following: **(10 x 2 = 20)**

a) Define terms Nibble and Byte related to binary number format.

b) Give expression for De-Morgan's 2nd Theorem.

c) Give two applications of multiplexers.

d) Specify the function of following IC's

IC 74138, IC 74139, IC 74154, IC 74155

e) Describe the procedure of converting D type flip-flop to T type flip-flop.

f) Draw 1 bit memory cell using NAND gate.

g) Define fan in and propagation delay related to logic families.

h) Why NOR gate is called as universal gate?

i) Give the significance of 74, 74H, 74L, 74S in IC numbering.

j) Give advantages of BCD code over other number codes.

k) Show that $\overline{(A+B)}\,(A+C) = \overline{A}C + AB$

l) State the rules for BCD addition.

Q2. Attempt any FOUR of the following: **(4 x 4 = 16)**

a) Subtract the given numbers using 1's &2's complement method

i) 25-17 ii) 17-25

b) Find complements of the following expressions using De Morgan's Theor

i) $F=\overline{X}\ \overline{Y} + \overline{XY}$ ii) $F=AB\overline{C}+A\overline{B}+A$

c) Give the expressions of gray code equivalent of 4 bit binary number using K-map.

d) What is race around condition in SR flip-flop? Describe the procedure to eliminate it.

e) Realize the following Boolean expressions using Basic Gates

(i) Y=ABC (ii) Y= (A+B) (C+D)

f) What are multiplexers? Give its advantages.

Q.3 Attempt any FOUR of the following: (4 x 4 = 16)

a) Identify the following as combinational or sequential logic circuits.

i) 2:1 multiplexer ii) SR flip flop

ii) Decode counter using T flip- flop. iv) 4 bit PIPO register.

b) Design the 3 bit Twisted ring counter. Explain its working with the help of wave forms.

c) Compare the propagation delay & power dissipation of TTL, ECL & COMS logic family.

d) Design 1:8 demux using 1:2 demux only.

e) What is a decoder? Explain how a demultiplexer can be used as a decoder.

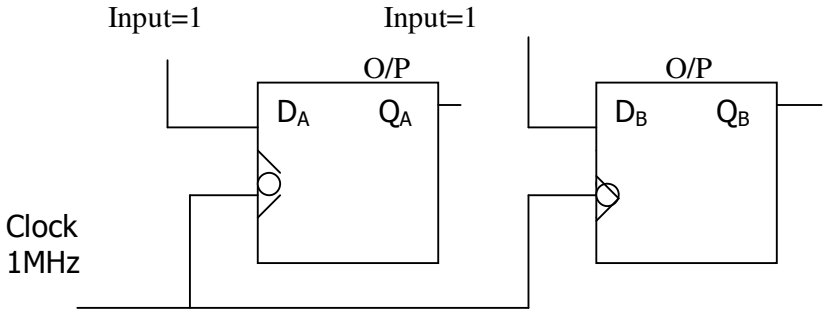
f) Explain the working of J-K Flip-Flop. Explain with logic diagram how it can be used as D Flip-Flop.

Q.4 Attempt any FOUR of the following: (4 x 4 = 16)

a) For a 3 bit SISO shift register draw the output waveform for following two conditions if input is 01010-

(i) Positive edge trigger (ii) Negative edge trigger.

b) Study the diagram given of PIPO register. Calculate the time required to get the output $Q_A Q_B = 11$



c) Compare CMOS and ECL families on the basis of basic gates, noise immunity, power dissipation and propagation delay.

d) Give any four characteristics of ECL family.

e) Realize following equation using demultiplexer

$f=\Sigma (0, 2, 5, 7, 8, 12, 15)$

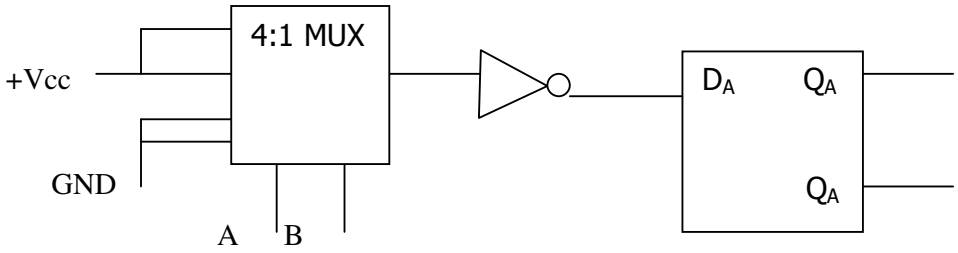
f) Realize Half Adder circuit using K-Map.

Q.5 Attempt any FOUR of the following: **(4 x 4 = 16)**

a) Convert BCD code from 0 to 3 into Excess – 3 code & gray code.

b) Describe with diagram 3 bit ring counter using D flip flop.

c) Write the truth table of the given diagram.



d) Minimize the following pos equation with k-map –

i) F = Σ m (0, 3, 5, 6, 9, 10, 12, 15).

ii) F = Σ m (0,1,2,3,11,12,14,15)

e) (i) Encode the following decimal numbers in Excess-3 code

a) 46 b) 327.79

(ii) Encode decimal number 46 to Gray code

f) Draw the block diagram of IC 7490 and explain its working as decade counter.

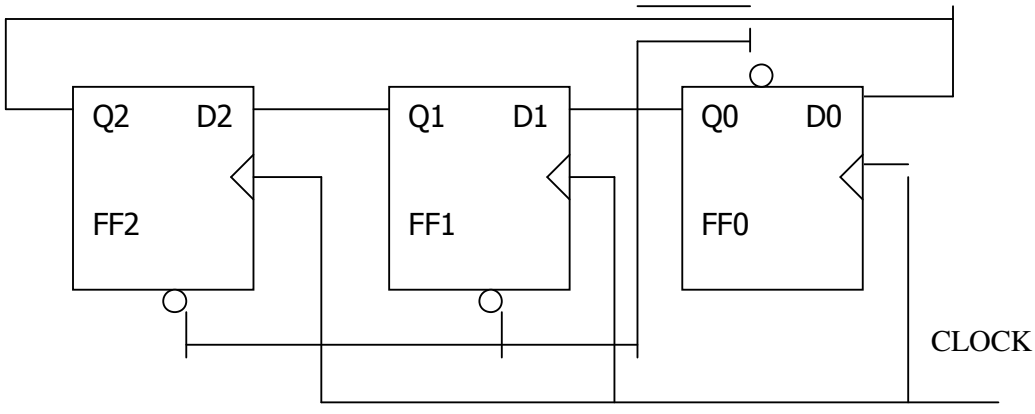
Q.6 Attempt any FOUR of the following: **(4 x 4 = 16)**

a) Draw the symbol for 2 input EX- NOR gate, write truth table & logical output equation.

b) Study the given diagram and

i) Specify which type of counter it is

ii) Design the truth table.



c) Design 3 bit PISO shift register using IC7474.

d) What is meant by decoder? Describe how demultiplexer can be used as decoders.

e) Explain the working of clocked S-R Flip-Flop with the help of logic circuit.

f) Draw the circuit and explain the principle of

(i) TTL NAND Gate (ii) TTL Gate with Totem pole output